



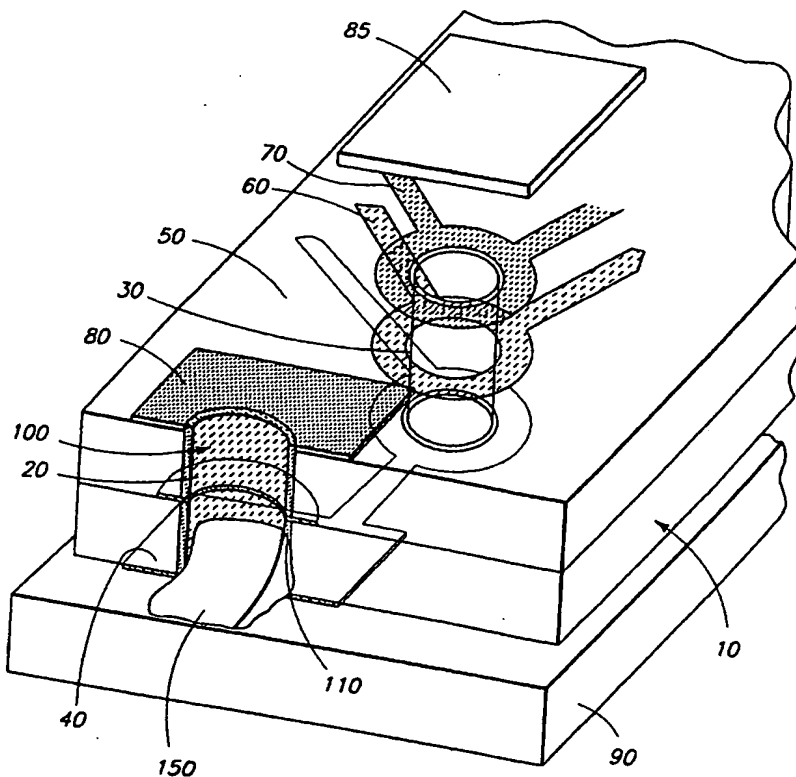
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(54) Title: PACKAGE FOR PROVIDING IMPROVED ELECTRICAL CONTACT AND METHODS FOR FORMING THE SAME

(57) Abstract

A package for connecting electrical components to a substrate is disclosed. The package includes conductive castellations around the perimeter of the package. The castellations are configured to electrically connect to the substrate, and to electrically connect to conductive features at an interior portion of the package. In turn, electrical components may be electrically connected to the castellations. The package may be used to form a module by electrically connecting the electrical components to the package and integrating the components by connecting various components or portions thereof to other components or portions thereof.



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PACKAGE FOR PROVIDING IMPROVED ELECTRICAL CONTACT AND METHODS FOR FORMING THE SAME

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FIELD OF THE INVENTION

The present invention generally relates to a package for integrating electronic components. More particularly, the present invention relates to an electronic component package for electrically coupling one or more electrical components to a substrate.

10

BACKGROUND OF THE INVENTION

Integration of one or more electrical components may be desirable for a variety of reasons. For example, it may be desirable to form a module that performs specific functions by integrating one or more electrical components such as microelectronic devices, inductors, capacitors, resistors, and the like. The modules may then be electrically attached to various substrates such as a printed circuit board (e.g., a motherboard for a computer), heat sinks, and the like.

The module generally includes a package configured to receive one or more electronic components and electrically attach to the substrate through conductive pads on a surface of the package. The package also typically includes a conductive path electronically connecting at least some of the components to at least some of the pads such that the connected components are electrically coupled to the substrate.

Using packages to integrate electrical components before the components are attached to the substrate may be advantageous because, among other reasons, fewer electrical connections between the substrate and the package are required than if each electrical component were individually attached to the substrate. Also, the substrate may require less complexity because the package may be configured to provide some integration of the electrical components, thus reducing the amount of integration required at the substrate level. Also, integration costs may be reduced if at least some of the components can be integrated using the package rather than the substrate.

30

Packages for providing electrical connections between various electrical components and the substrate and methods for forming the packages are generally known in the art. For example, leadframe packages may be used to electrically connect one or more electrical components to the substrate. Modules including leadframes generally

include one or more electrical components attached to the leadframe and several conductive leadframe pins that serve as electrical contacts between the components and the substrate. Typically, the leadframe module is attached to the substrate by soldering the leadframe pins to conductive bond pads resident on the substrate or the like.

5 Using leadframes to form electrical contacts between the electrical components and the substrate may be disadvantageous for several reasons. For example, it may be expensive to add leadframes to the respective modules. Also, the addition of the leadframe tends to increase the overall size of the module, which can increase material and fabrication labor costs associated with module manufacturing. Also, at high
10 frequencies (e.g., RF) the leadframe pins may cause high inductance for the module; such high inductance may degrade module performance or performance of the electronic components attached thereto.

 Modules (including leadless chip carrier (LCC) packages) to electrically connect one or more electronic components to the substrate are also known in the art. The LCC
15 package may include several conducting and insulating layers, wherein the conducting layers of the LCC may be connected to the electrical components, other conducting layers of the LCC, and conductive bond pads attached to the LCC to integrate the components and couple them to the substrate. Typically, the module, and consequently the electronic components, are coupled to the substrate by placing the bond pads of the LCC over
20 solder pads of the substrate and causing conductive material (e.g., solder) to attach to both the LCC and the substrate.

 One method for attaching the LCC module to the printed circuit board and forming electrical contacts between the module and the circuit board includes forming conductive castellations around the perimeter of the LCC and applying conductive material such as
25 solder or conductive epoxy to the conductive castellations and the substrate solder pads. In addition to providing electrical contact to the substrate, the conductive castellations also suitably provide a conductive path between electrical components attached to the LCC and the substrate, the various conductive layers of the LCC, and the like.

 The conductive castellations on the LCC are generally formed by drilling or
30 punching holes through the LCC to form cylindrically-shaped vias, applying a conductive surface to the interior portion of the vias, and sawing or cutting through the vias to expose a portion of the via, thereby creating semi-cylindrical, conductive features around the perimeter of the LCC module.

Modules (including LCC packages) that have conductive castellations about the module's perimeter may be advantageous for several reasons. In particular, high inductance problems associated with leadframe packages are reduced because the LCC package is attached directly to the substrate, thus reducing the conductive path length between the module and the substrate and the associated inductance. Packages including conductive castellations may also be advantageous because test pads electrically connected to the castellations may be conveniently formed on a surface (e.g., a top surface) of the module. These test pads may be used to measure or test for continuity between the castellations of the package and the bond pads of the substrate and to test the electrical performance of the module and components attached thereto. Also, the conductive castellations of the device may be used to electrically connect two or more conductive layers within the LCC without additional device fabrication steps. In addition, using castellations to form electrical contact between the LCC device and the printed circuit board allows relatively easy visual inspection of the device's electrical connections between the module and the printed circuit board because the electrical connections are formed at the outside edge of the module. In other words, the integrity of the electrical connections between the conductive castellations and bond pads on the printed circuit board may be electrically and visually checked relatively easily because the contact is formed at the perimeter of the module.

Although packages including castellations are advantageous in some respects, these packages also have several shortcomings. For example, conductive castellations may not provide a reliable conductive path between the electrical components and the substrate, between various conducting layers of the package, and the like. The unreliability may be due to the sawing or cutting across the vias during castellation formation, which may cause the conductive surface initially attached to the interior portion of the vias to delaminate or to become stressed and susceptible to delamination. Conductive surfaces that have become stressed may delaminate due to, for example, temperature cycling which may occur during module use. The delamination of the conductive surface may create electrical opens in the castellations of the LCC module. Electrical opens in the castellations of the module may in turn create electrical opens between the electrical components attached to the package and the bond pads on the printed circuit board, between various conductive layers of the package, and the like.

An LCC package may alternatively include solder contacts or the like at an interior portion of the package, that is, away from the perimeter of the package, and use conductive features, located at an interior portion of the package, to electronically connect various conductive layers of the package and electrical components attached thereto to the substrate. The solder contacts of the package are typically in the form of conductive pads or balls; accordingly, the module including the LCC package having internal conductive pads is often referred to as a ball grid array module. The pads of the ball grid array module are generally configured to electrically couple to bond pads on the substrate surface.

Ball grid array modules may be advantageous because the interior conductive features may be more reliable than conductive castellations. In contrast to castellations, the conductive elements of the ball grid array module are not sawed or otherwise cut; therefore, the conductive features remain generally intact during package formation. Consequently, the conductive features of the module and electrical connections made thereby are less susceptible to conductive material delamination and resulting electrical opens.

Ball grid array modules may, however, also suffer from several shortcomings. In particular, the integrity of electrical contacts between the module and the substrate may be difficult to determine because the contact between the ball or contact pad of the module and the bond pad of the substrate is difficult to visually inspect (as mentioned above, the electrical contact is not formed at the outside edge of the module). Also, continuity and other electrical measurements between the module and the printed circuit board may be difficult to test or measure because the package typically does not include test pads electrically connected to the conductive features.

Therefore a package that overcomes the shortcomings associated with prior art packages used to connect various electrical components to a substrate and methods for forming the same are required.

SUMMARY OF THE INVENTION

The present invention provides a package having improved electrical contacts for electrically coupling the package to a substrate and for electrically coupling the package to electrical components. While the way in which the present invention addresses the

drawbacks of now known packages will be described in greater detail below, in general, in accordance with various aspects of the present invention, the inventive package provides improved electrical contacts that are reliable and easy to visually or otherwise inspect.

5 In accordance with the present invention, the package includes conductive castellations configured to electrically connect to conductive portions of the substrate and conductive features at an interior portion of the package. The conductive features are configured to electrically connect electrical components attached to the package and conductive layers of the package to the castellations.

10 In accordance with other aspects of the present invention, the castellations are electrically connected to bond pads on a lower surface of the package, and the package bond pads are configured to electrically connect to conductive portions of the substrate.

In accordance with other aspects of the present invention, test pads may be electrically connected to the castellations to allow continuity and other electrical
15 measurements of a module including the package.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the
20 figures, wherein like reference numbers refer to similar elements throughout the figures, and:

Figure 1 is an exploded view of a portion of an exemplary package and a portion of a substrate; and

Figure 2 is a perspective view of a portion of an exemplary package attached to a
25 substrate.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

30 The present invention generally relates to an apparatus for connecting electronic components, such as, for example, integrated circuits, resistors, capacitors, and the like, to a substrate. Although the inventive apparatus may include a variety of forms, the present invention will generally be described herein below as a package having one or

more conductive layers configured to couple to the electronic components. However, the inventive apparatus may suitably include an integral, solitary unit without extrinsic electrical components attached thereto. The solitary unit may then be attached to the substrate.

5 Referring now to Figures 1 and 2, a portion of a package 10 in accordance with a preferred embodiment of the present invention is shown. As described in greater detail herein below, package 10 is preferably configured to provide reliable electrical contacts to the electrical components attached to package 10 and to provide electrical contacts that are relatively easy to visually inspect.

10 In accordance with preferred embodiments of the present invention, package 10 includes a castellation 20, a conductive feature 30, and a contact pad 40. Package 10 also suitably includes conductive layers such as conductive traces 50, 60, 70 and a test pad 80. The various conductive layers are typically separated by a suitable insulating material, or a dielectric composition such as ceramic or glass materials, silicon materials,
15 and the like.

Although partial package 10 shown in Figures 1 and 2 illustrates one castellation 20, one conductive feature 30, one contact pad 40, and one test pad 80, those skilled in the art will appreciate that package 10 may include any number of castellations 20, features 30, bond pads 40, test pads 80, and the like wherein the number of each element
20 is generally determined by the module function and complexity. Furthermore, the specific configuration, size, and interconnecting arrangement of the conductive elements may vary from application to application.

Package 10 is generally configured to receive several electronic components on at least one surface of package 10 and to provide electrical connections between at least
25 some of the components and a substrate 90. The components are typically selected such that when the components are attached to package 10 and integrated with each other (e.g., by traces 50, 60, 70 and features 30 of package 10), the combination of the components (e.g. a semiconductor die 85) and package 10 forms a module that can be mechanically attached and electrically connected to substrate 90. In accordance with
30 alternative embodiments of the present invention, package 10 may include electrical components, such as resistors, capacitors, inductors, and the like, integral with package 10. Such integral components may be formed on the surface of package 10, interior to package 10, or any combination thereof.

As will be described in more detail below, an electrical path connecting the components to substrate 90 generally includes castellations 20, conductive features 30 (which generally connect various conductive layers of package 10), package bond pads 40, and conductive layers such as traces 50, 60, 70. Using both features 30 and
5 castellation 20 to form an electrical path between the components and substrate 90 provides a relatively reliable path that is relatively easy to visually inspect. In particular, the path is reliable because the paths between various layers of package 10 are formed in an interior position of package 10. The contact is relatively easy to inspect because the contact is formed at castellation 20 on the perimeter of package 10.

10 A specific conductive path for the component or portion thereof varies from application to application. However, in general, the path includes a conductive layer coupled to the component (e.g., die 85) and feature 30, a conductive layer such coupled to feature 30 and Contact Pad 40, and conductive material coupled to pad 40 and substrate 90. In accordance with particularly preferred embodiments of the present
15 invention this conductive path joining features 30 and contact pad 40 is formed at a bottom portion, and more preferably on a bottom surface 95 of package 10. Forming the electrical connection between pad 40 and feature 30 on bottom surface 95 creates a particularly reliable connection between the component and bond pad 40.

Protective insulating material (not shown) may be added to package 10 to prevent
20 unwanted electrical shorting or the like. In accordance with preferred embodiments of the present invention, insulating material such as solder mask is applied to surface 95 of package 10 to prevent unwanted electrical shorting between conducting layers (e.g. trace 50) of package 10 and conducting portions of substrate 90.

The function and arrangement of substrate 90 may vary according to the particular
25 application. For example, substrate 90 may be configured to provide package 10 and the module with a heat sink. Alternatively, substrate 90 may include ceramic material or a laminated board such as a printed circuit board configured to perform various electronic functions. As described in more detail below, the various configurations of substrate 90 suitably include conductive portions configured to facilitate electrical coupling between
30 substrate 90 and package 10.

To facilitate mechanical attachment and electrical connection between package 10 and substrate 90, package 10 includes castellation 20 about the perimeter of package 10. Castellation 20 generally includes a depression 100 on the perimeter of package 10 and

a conductive material 110 attached to or integral with depression 100. Although conductive material 110 may be integral with depression 100, in preferred embodiments of the present invention, conductive material 110 is coated or deposited onto the surface of depression 100.

5 Depression 100 may be in any form; however, depression 100 is preferably substantially partial or semi-cylindrical and spans substantially the entire height of package 10. In a particularly preferred embodiment of the present invention, the radius of the substantially cylindrical portion is approximately 10 mils before depression 100 is coated with material 110, and depression 100 may be coated with, for example,
10 approximately 1 mill of conductive material 110. However, the shape and size of castellations 20 may vary according to the specific configuration and/or function of package 10. For example, it may be desirable to have fewer and/or larger castellations for a particular application.

 Conductive material 110 may include a variety of one or more materials and be
15 coated, deposited, or the like onto or into depression 100 in a variety of ways. In preferred embodiments of the present invention, conductive material 110 includes material that is wettable to materials used to mechanically bond and electrically connect package 10 to substrate 90. Such materials preferably include metals and are preferably deposited onto depression 100 by plating material 110 onto the exposed surface of depression 100.
20 However other methods of depositing materials, including physical and chemical vapor deposition methods may suitably be used to deposit various films to form conductive material 110. In particularly preferred embodiments of the present invention, copper or gold is plated onto depression 100.

 Conductive material 110 may include multiple films, and the films may perform
25 various functions. In particular, to assist coating depression 100 with material 110 and improve adhesion of material 110 to depression 100, conductive material 110 may include a seed layer (not shown) applied to depression 100. For example, if conductive material 110 includes electroplated copper, the seed layer preferably includes electroless copper. Conductive material 110 may also include additional layers of nickel, gold, or the like to
30 enhance wetting between conductive material 110 and material which forms a bond between castellation 20 and substrate 90.

 Castellation 20 may be formed in a variety of ways. In accordance with preferred embodiments of the present invention, castellation 20 is formed by drilling, punching,

etching, or otherwise creating vias proximate the perimeter of package 10. The vias are then typically coated with conductive material 110. As noted above, the vias are preferably coated with conductive material 110 by depositing electroless and electrolytic copper onto the surfaces of the vias. In particularly preferred embodiments of the present invention, the vias are coated by immersing package 10 in an electroless copper bath to coat package 10 with approximately 1 microinch of copper. Package 10 may then be placed in an electrolytic copper bath to plate approximately 1 mil of copper onto package 10. The copper may then be patterned and etched, using methods now known or hereafter devised by those skilled in the art, leaving the vias, and if desired, other portions of package 10 coated with copper. In addition, conductive traces, electrical components, or a combination thereof may also be formed on the surface of package 10 during the patterning and etching steps of conductive castellation 20 formation.

After the via has been formed and coated with conductive material 110, castellation 20 may be formed by sawing or otherwise cutting through the via to form a substantially semi-cylindrical or substantially partial-cylindrical, conductive castellation 20. In an alternate embodiment of the present invention, castellation 20 may be formed by coating depression 100 with conductive material 110 after the vias are cut to form castellations 20.

Although depression 100 described above is formed by cutting through a substantially cylindrical via, those skilled in the art will appreciate that the via may be of any suitable shape. For example, package 10 surface may be patterned with a square or other geometric shape, and the via may be formed by etching package 10 material to form a via with a corresponding cross section.

Conductive feature 30 is generally configured to form part of an electrical path between the component and substrate 90. As noted above and in accordance with the preferred embodiment of the present invention, conductive feature 30 is located at an interior portion of package 10 to increase reliability of the electrical path between the components, various conductive layers of package 10, and contact pad 40.

Feature 30 may also be suitably configured to facilitate integration of one or more electronic components electrically connected or integral to package 10. Electrical integration may be obtained by electrically connecting the components or portions thereof to other components or portions thereof through conductive layers (e.g., traces 50, 60, 70) of package 10 and coupling at least a portion of the conductive layers to at least a portion of conductive features 30. The electrical components are typically attached and

electrically connected to the surface of package 10 by attaching the component to bond pads (not shown) that may be suitably attached to or integrated with, for example, trace 70. The components or portions thereof may then be suitably integrated by electrically coupling at least a portion of a first component to conductive feature 30 and connecting at least a portion of a second component to the same conductive feature 30 and the like. Although not shown in the figures, any number of conductive layers may be electrically coupled to any number of features 30. For example, one conductive feature 30 may be electrically coupled to traces 50, 60, 70 and other features 30 may be connected to various subsets of electrical traces 50, 60, 70 or other conductive layers.

Although conductive layers such as traces 50, 60, 70 and electrical components (e.g., die 85) attached to package 10 may be electrically connected to each other through castellation 20, according to preferred embodiments of the present invention, package 10 need not solely rely on castellation 20 as an interconnecting element. Rather, as noted above, various conductive layers of package 10 are preferably connected to each other using features 30. Consequently, the reliability of electrical paths connecting the conductive layers and the electrical components to substrate 90 are not dependent on the structural and electrical integrity of castellation 20. Nevertheless, as described in more detail below, it is preferable to have castellation 20 substantially intact, at least prior to module attachment to substrate 90, because, among other reasons, a substantially intact castellation 20 may enhance adhesion of materials used to attach package 10 to substrate 90. In addition, castellation 20 provides a conductive path that allows electrical testing of various electrical connections of package 10.

Conductive feature 30 may be formed during and in similar fashion to castellation 20 formation. In general, conductive feature 30 is formed by creating a via by drilling, etching, or the like through at least a portion of package 10. As described in more detail below, conductive feature 30 is typically configured to penetrate through one or more conductive layers such as traces 50, 60, 70 such that the conductive layers may be electrically connected to form a conductive path between the layers and components attached to package 10. Similar to castellation 20, conductive feature 30 typically includes a substantially conductive material surrounding the via. In preferred embodiments, conductive feature 30 includes about one microinch of electroless copper and about one mil of electroplated copper.

As noted above, conductive layers such as traces 50, 60, 70 may be used to integrate one or more electronic components attached to or integral with package 10 or to electrically connect features 30 to bond pads 40. Preferably, the conductive layers are formed from materials with relatively low electrical resistance such as metals and the like.

5 In particularly preferred embodiments of the present invention, the conductive layers include traces of patterned copper metal. The conductive layers may be formed by any now known or hereafter developed method. For example, the layers may be formed by plating the conductive material onto a surface of package 10, patterning the conductive material with a composition resistant to an etchant, and etching the conductive material
10 with the etchant.

The conductive layers may include a variety of forms. Preferably, at least a portion of the conductive layer includes a via pad 130, which is electrically connected to at least one conductive feature 30 of package 10. Package 10 may include any number of conductive layers, which number is usually determined by the module's level of
15 component integration. As stated above, not all conductive layers need to be electrically connected to all conductive vias 30 of package 10. For example, conductive layers such as traces 60, 70 may not include via pads 130 connected to one or more conductive features 30.

The conductive layers of package 10 are typically coupled to various features 30,
20 during the formation of features 30, by drilling through a portion of the conductive layer such as via pad 130 and coating the drilled portion with conductive material to form conductive feature 30. In other words, the conductive layers are electrically coupled to features 30 by forming a conductive intersection between the layer and various features 30. For example, conductive trace 50 may be electrically coupled to feature 30 by forming
25 a via through pad 130 connected to trace 50 and applying conductive material to pad 130 and the via.

Conductive layers may also connect features 30 to bond pad 40. In accordance with a preferred embodiment of the present invention, a conductive layer connecting pad 40 to feature 30 including via pad 130 and trace 50.

30 An electrical connection between package 10 and substrate 90 is generally formed to electrically couple castellation 20, Contact Pad 40, and a bond pad 140 of substrate 90. Contact Pad 40 may be formed from a variety of materials and may be located at various locations on the surface of package 10. In accordance with preferred embodiments of the

present invention, pad 40 is formed of conductive material such as copper and is located on a bottom portion of package 10, and more preferably at the bottom perimeter of package 10. In addition, while Contact Pad 40 may be in the form of various shapes such as partial spheres and the like, pad 40 is preferably formed in a shape having a substantially rectangular cross section.

Typically, package 10 is electrically and mechanically attached to substrate 90 by aligning castellation 20 over bond pad 140 and applying conductive material or otherwise forming an electrical connection between castellation 20 and bond pad 140. For example, a piece of solder 150 may be used to attach package 10 to substrate 90 as well as electrically connect castellation 20 to bond pad 140. In accordance with preferred aspects of the embodiment of the present invention, a portion of solder 150 is placed between pad 40 and pad 140 to assist mechanical attachment of package 10 to substrate 90. Alternatively, bond pad 140, Contact Pad 40, or a combination thereof, may include solder or similar material which when heated, pressed against another conductive surface, or the like, forms a mechanical attachment and an electrical connection between substrate 90 and package 10. In yet a further embodiment of the present invention, conductive epoxy or the like may be used to mechanically attach and electrically connect package 10 to substrate 90.

As noted above, conductive material 110 of castellation 20 preferably includes material that is wettable with respect to the material, such as solder or epoxy, used to attach package 10 to substrate 90. If the attachment material wets conductive material 110, the attachment material will generally adhere to conductive material 110 and be drawn up by capillary forces toward top surface 120 of package 10 as the material wets castellation 20. Solder piece 150, which wets conductive material 110 and is drawn up castellation 20, is illustrated in Figure 2.

Forming an electrical connection and a mechanical attachment between package 10 and substrate 90 at castellations 20, and more particularly at castellations 20 located at the perimeter of package 10, allows a person to visually inspect the electrical connection between package 10 and substrate 90. In particular, the person may be able to determine whether castellation 20 is correctly aligned over bond pad 140, whether solder piece 150 was properly applied to both castellation 20 and bond pad 140, whether solder 150 wetted and adhered to castellation 20, and the like.

Package 10 may also include test pads 80 electrically connected to castellation 20 to allow the person to readily test for or measure continuity or other electrical parameters between various locations of package 10, between various locations of package 10 and various locations on substrate 90, any combination thereof, and the like. Accordingly, test pad 80 may be located on any surface of package 10, as long as test pad location 80 allows the user to make desired electrical measurements. In a preferred embodiment of the present invention, test pad 80 is located on a top portion, and more preferably on top surface 120 of package 10. In a particularly preferred embodiment of the present invention, pad 80 is proximate castellation 20. Placing pad 80 near castellation 20 may provide an additional benefit of increasing adhesion of conductive material 110 to depression 100.

The terms top, bottom, and the like have been used throughout this application to refer to various directions or portions of the apparatus. These terms are used for reference to the drawing figures only and are not meant to limit possible configurations of the apparatus described hereinabove. In addition, although the present invention is set forth herein in the context of the appended drawing figures, it should be appreciated that the invention is not limited to the specific forms shown. For example, the device may include various numbers of conductive layers, features, and castellations, depending on the intended use for the apparatus. Various other modifications, variations, and enhancements in the design and arrangement of the device as set forth herein may be made without departing from the spirit and scope of the present invention as set forth in appended claims.

CLAIMS

What is claimed is:

- 5 1. A package for electrically coupling to an electronic component to form a module, said package comprising:
 a conductive castellation formed at the perimeter of the module;
 a conductive layer on a bottom portion of said package electrically coupled
to said castellation; and
10 a conductive feature electrically coupled to said conductive castellation.
2. The package of claim 1 further comprising a contact pad electrically connected to said castellation.
- 15 3. The package of claim 2 wherein said contact pad is located at a bottom portion of said package.
4. The package of claim 1 further comprising a test pad electrically connected to said castellation.
20
5. The package of claim 4 wherein said test pad is located at a top portion of said package.
6. The package of claim 1, wherein said package comprises a plurality of
25 conductive layers, and wherein at least a portion of said plurality of conductive layers are electrically coupled to said conductive feature.
7. The package of claim 1 further comprising a conductive layer on a surface of the package electrically connected to the electronic component.
30
8. A method of forming a package for an electronic module, the method comprising the steps of:
 forming an interior via at an interior portion of said package;

adding a conductive material to said interior via;
producing a conductive castellation in said package, said castellation being
electrically coupled to said conductive material; and
forming a conductive path between said conductive material and said
5 castellation at a lower portion of said package.

9. The method of claim 8 further comprising the steps of:
forming a conductive trace interior to said package; and
electrically connecting said interior conductive trace to said conductive
10 material.

10. The method of claim 9 further comprising the step of forming a contact pad
on a surface of said package.

15 11. The method claim 10 further comprising the step of forming an electrical
connection between said contact pad and said castellation.

12. The method claim 8 further comprising the step of forming a test pad on a
surface of said package, wherein said test pad is electrically connected to said
20 castellation.

13. A module for integrating a plurality of electrical components, the module
comprising:

25 a package having a plurality of conductive features located at an interior
portion of said package and a plurality of conductive castellations electrically connected
to at least a portion of said plurality of conductive features;

a conductive trace on a bottom portion of said package electrically
connected to at least one of said conductive castellations; and

a substrate electrically connected to said conductive castellations.

30 14. The module of claim 13 further comprising a conductive layer internal to said
package, said conductive layer being electrically connected to at least one of said
conductive features.

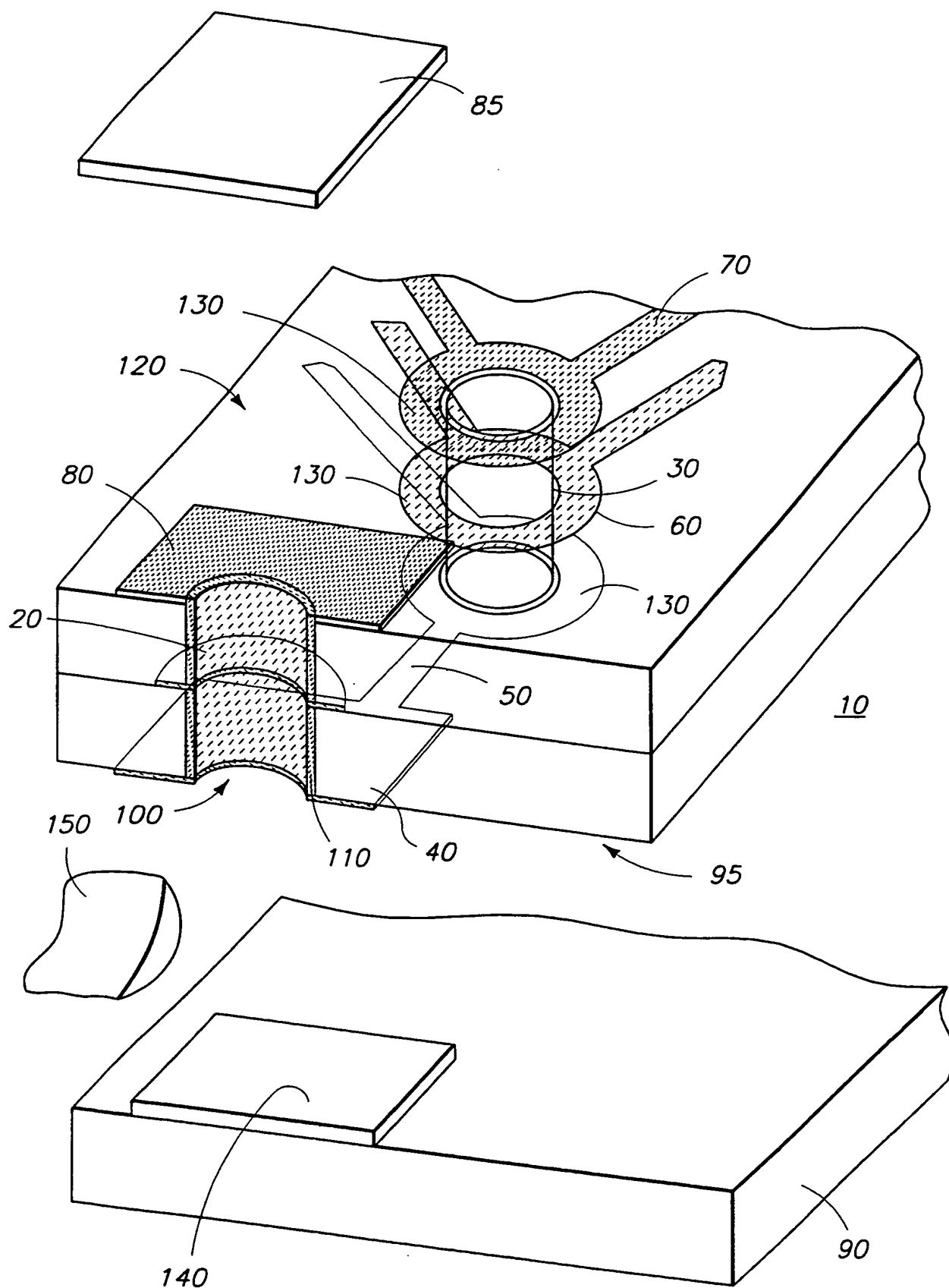


FIG. 1

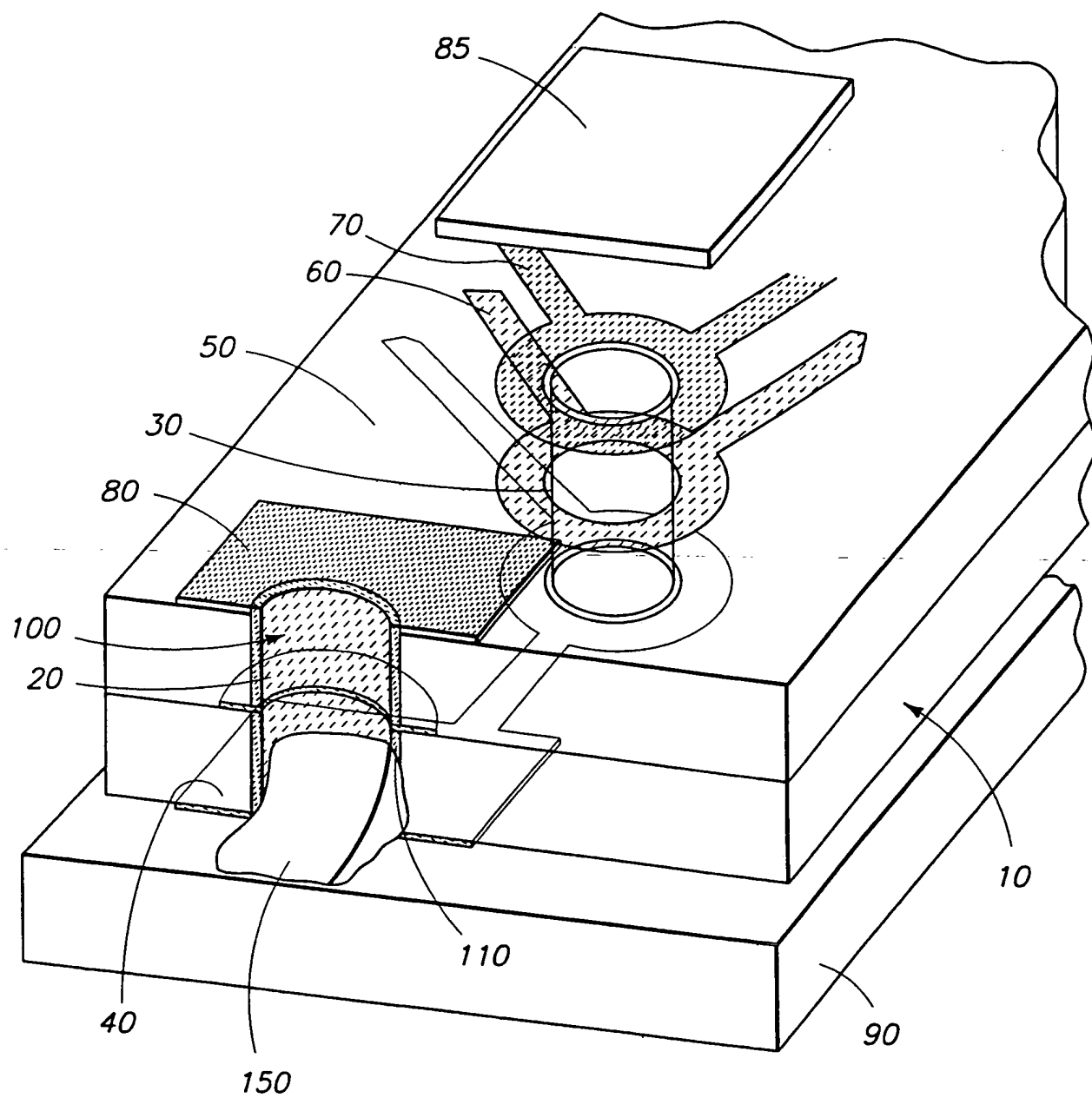


FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/14800

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L23/498

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WEINBERG A ET AL: "PROCEEDINGS OF THE ELECTRONIC COMPONENTS CONFERENCE, LOS ANGELES, MAY 9 - 11, 1988" PROCEEDINGS OF THE ELECTRONIC COMPONENTS CONFERENCE, LOS ANGELES, MAY 9 - 11, 1988, no. CONF. 38, 9 May 1988 (1988-05-09), pages 436-444, XP000013845 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS ISSN: 0569-5503 figures 4,5	1-14
X	US 4 551 746 A (GILBERT BARRY K ET AL) 5 November 1985 (1985-11-05) abstract; figures 1,25 column 10, line 11 - column 11, line 17 column 14, line 21 - line 39 --- -/--	1-4,6-12

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

12 October 1999

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/14800

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 564 865 A (MOTOROLA INC) 13 October 1993 (1993-10-13) abstract; figure 4 ---	4,5,12
A	US 5 314 606 A (IRIE TAKA ET AL) 24 May 1994 (1994-05-24) figure 3B column 2, line 34 -column 3, line 18 -----	8-12

INTERNATIONAL SEARCH REPORT

information on patent family members

International Application No

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